REMARKS

Claims 18 through 20, 24 and 25 remain pending. Applicants respectfully traverse the rejections set forth in the Office Action and request reconsideration. Applicants also wish to thank the Examiner for the withdrawal of the 35 U.S.C. § 112 rejection.

Claims 18 – 20, 24 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,727,171 (issued Mar. 10, 1998) to Iachetta, [hereinafter "Iachetta"], in view of U.S. Patent No. 6,141,715 (issued Oct. 31, 2000) to Porterfield, [hereinafter "Porterfield"], U.S. Patent No. 5,859,988 (issued Jan. 12, 1999) to Ajanovic, et al [hereinafter "Ajanovic"] and U.S. Patent No. 5,392,407 (issued Feb. 21, 1995) to Heil et al. [herinafter "Heil"].

Applicants respectfully note that it appears that Applicants' prior amendments were overlooked and perhaps misapprehended. Applicants have previously amended claim 18 with inherent language indicating that the I/O controller is in communication with high speed Bus arbiter that is in the system controller and is also in communication with a separate Bus that is not coupled to the low speed Bus arbiter and is coupled to a data storage device. In the "Response to Arguments" starting on page 8 of the Office Action, it appears that the same remarks were cut and pasted from a prior response, except for a sentence that is on page 11 a portion of which is underlined. Therefore the "Response to Arguments" section still includes, from the prior response, statements such as "[n]ote also that the word "coupled" does not mean a direct connection" (page 10) and that..."with the PCI specification, [it] is "coupled" to the PCI/bridge 810..." (page 11). Applicants respectfully note that the words "coupled to" were removed from claim 18 in the previous Amendment. Therefore these statements are no longer applicable to the instant claims.

Moreover, the Office Action on page 7 states that "the memory bus 650," which is shown in Iachetta Fig. 4, and is only coupled to the host bridge 640 and the memory subsystem 660, "is not coupled to the low speed bus arbiter 910 and coupled to the storage device 660" in an attempt (apparently) to read on the claim language referencing the claimed I/O controller and the separate bus connection. However the claim indicates that the claimed I/O controller is in communication not only with the high speed bus arbiter via a high speed bus, but is also in communication with a separate bus (for example bus 133 to hard drive 150 as shown in Applicants' FIG. 1) that is not coupled to the low speed bus arbiter and [is] coupled to a data storage device. Iachetta shows distinctly different structure, and the memory bus 650 apparently alleged to correspond to the claimed "separate bus" is in fact not coupled to the PCI to PCI Bus Bridge 810 of Iachetta, as it would need to be coupled based on the corresponding structure identified by the USPTO to correspond to the claimed I/O controller. Since the claimed structure is patentably distinguishable from the structure disclosed by Iachetta, this reference does not teach what is alleged and Applicants respectfully submit that the claim is in condition for allowance.

Claims 19 and 20, being dependent claims depending from, and including all features of independent claim 18, are likewise in condition for allowance. Likewise claim 24, which was rejected based on the discussion with respect to claim 18 is in condition for allowance. Reconsideration and withdrawal of the rejections of claims 18 through 20 and 24 is respectfully requested.

Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Iachetta, in view of Porterfield, Ajanovic, and Heil as applied to claims 18-20 and further in view of (apparently) Wikipedia articles about North Bridge and South Bridge.

With regard to claim 25, this claim is a dependent claim which includes all the features of independent claim 24 and is therefore allowable for the reasons provided above. Further, claim 25 requires a dual bus based unified memory architecture wherein a unified memory is controlled to store both graphics data and system data. Applicants respectfully note that Heil, which was cited in the Office Action as disclosing "two separate memory channel controllers," does not discloser a unified memory as required by claim 25. See Office Action, page 6. Heil specifically discloses two separate memory elements, as in Heil FIG. 8 "code/data storage 138" and "frame buffer 140." There is no "unified memory" disclosed in Heil and therefore claim 25 is also allowable for this feature.

Reconsideration and withdrawal of the rejection of claim 25 is respectfully requested.

Accordingly, Applicants respectfully submit that the claims are now in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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By: /Joseph T. Cygan/
Joseph T. Cygan
Reg. No. 50,937

Vedder Price, P.C.
222 North LaSalle
Chicago, Illinois 60601
312/609-7945
312/609-5005 Facsimile